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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant	:	Tongbi Jiang
Appl. No.	:	09/471,071
Filed	:	December 21, 1999
For	:	DIE ATTACH MATERIAL FOR TBGA OR FLEXIBLE CIRCUITRY
Examiner	:	Jose Alcala

Group Art Unit 3763

I hereby certify that this correspondence and all marked attachments are being deposited with the United States Postal Service as first-class mail in an envelope addressed to: United States Patent and Trademark Office, P.O. Box 2327, Arlington, VA 22202, on

March 8, 2002
(Date)

Sabing H. Lee, Reg. No. 43,745

AMENDMENT

United States Patent and Trademark Office
P.O. Box 2327
Arlington, VA 22202

Dear Sir:

In response to the Office Action dated December 10, 2001, please amend the above-identified application as indicated below.

IN THE SPECIFICATION:

Please amend the paragraph at page 6, line 22 as follows:

A1

FIGURE 1C shows a fragmentary cross-sectional view of an alternate embodiment in which the leads 50 are located on the same side as the terminals 40; thus, not requiring the conductive vias 70 (shown in **FIGURE 1B**). A solder mask/coverlay is also used in the embodiment shown in **FIGURE 1C** because the leads 50 and the terminals 40 are on the same side of the substrate 30. The solder mask/coverlay provides a dielectric coating ensuring that the solder connecting the terminals to contacts on the printed circuit board does not wick down the leads or short to other soldered terminals.

Please amend the paragraph at page 8, line 3 as follows:

A2

A die attach material 80' is provided over the die 10, and a solder ball array 40 is provided over the die attach material that serves to make the connection to the next-level package. The solder balls 40 are preferably relatively flexible and can thus compensate for any lack of flatness in the printed circuit board or package. Additionally, the solder balls are assembled in an array, and thus provide a relatively high throughput. In one preferred embodiment, the solder balls are made of a SnPb eutectic material such as Sn63Pb37 and have a diameter of about 0.3 to 0.5 mm. The bump pitch on the tape can be as small as about 0.25 to 1 mm, and is more preferably about 0.5 mm.

Please amend the paragraph at page 8, line 12 as follows:

A3

Tape 50' extends over the die attach material forming a connection with the solder ball array 40. TAB leads 55' extend from the tape 50' to form a connection with the die 10 at die pads 20. The tape 50' preferably comprises a conductive material such as copper for connecting a die pad 20 to a solder ball 40, and a polyimide material to connect the solder balls. The tape 50' preferably has a thickness of about 50 μm.

Please amend the paragraph at page 8, line 17 as follows:

A4

FIGURE 3 illustrates in cross-section a close-up view of the first level package 8 of **FIGURE 2**. Leads 55' are preferably ultrasonically bonded to the die 10 at die pads 20 (not shown). The point where the leads 55' contact the die 10 is the heel 86.

Please amend the paragraph at page 8, line 20 as follows:

A5

The die attachment layer 80' can be made from an epoxy modified with elastomeric material used to prevent breakage of the leads 55' from the die 10 at the heel 86 (the heel break). The thickness of the layer is preferably about 3 to 9 mils, more preferably about 5 to 7 mils. In one embodiment, the die attachment layer has a modulus of elasticity of about 126 ksi at room temperature. This die attachment layer preferably has a glass transition temperature T_g of about 42°C, a coefficient of thermal expansion (CTE) of about 106 ppm/°C or less below T_g, and a CTE of about 234 ppm/°C above T_g. Such a material is available from Ablestik Lab of Rancho Dominguez, California, No. RP 559-2A.

Please amend the paragraph at page 9, line 4 as follows:

A6

For instance, the die attach layer 80' is designed to have a low CTE in order to minimize the amount of expansion and contraction of the layer, especially relative to the die 10 and the tape 50', thereby preserving the connection between the die 10 and the leads 55' at the heel 86. This is important because the package 8 may undergo temperature cycling, for example, between -55 and 125°C, for up to 1000 cycles or more.

Please amend the paragraph at page 9, line 10 as follows:

A7

In one embodiment, the die or chip 10 has a CTE of about 3 ppm/°C and the tape 50' has a CTE of about 20 ppm/°C. The CTE of the tape 50' is the "effective CTE" of the combined layers forming the tape. Thus, as compared to the prior art, it has been discovered that a die attach layer 80' with a CTE closer to that of the die and the tape is desirable, preferably less than 200 ppm/°C, more preferably less than 150 ppm/°C. In the embodiment described above, it has been found that a CTE of less than about 100 ppm/°C is sufficient to alleviate the heel break problem. The reduced movement of the die attach layer 80' because of the low coefficient of thermal expansion reduces the risk of breakage of the leads 55' at the heel 86.

Please amend the paragraph at page 9, line 19 as follows:

A8

While the die attach layer preferably has a low coefficient of thermal expansion, the present inventors have found that the layer should still be sufficiently compliant to absorb stresses between the die 10 and the solder balls 40. However, as compared to the prior art, in one embodiment, the modulus of elasticity of the die attach layer 80' is selected to be higher than that of previous die attach layers. Thus, wherein some prior art die attach layers have a modulus of less than 10 ksi, one embodiment of the present invention provides a die attach layer with a modulus of greater than about 10 ksi, more preferably greater than about 50 ksi, even more preferably greater than about 100 ksi, and in one embodiment, up to about 126 ksi. The higher modulus provides improved resistance to movement in the die attach layer, thereby decreasing the amount of stress concentrated at the heel 86. At the same time, the modulus of the layer 80' is still sufficiently compliant to reduce the amount of stress applied to the solder balls 40.

IN THE CLAIMS:

Please cancel Claims 1-7 and 24 without prejudice.

Please amend the claims as follows:

8. An integrated circuit package, comprising:

a die;

a die attach layer over the die; and

an array of solder balls over the die attach layer;

wherein the die attach layer has a coefficient of thermal expansion of less than about 106 ppm/°C.

a9

9. (Amended) The integrated circuit package of Claim 8, further comprising a flexible tape connecting the array of solder balls to the die, wherein one end of the tape is located over the die attach layer, and another end of the tape is located over the die.

10. The integrated circuit package of Claim 8, wherein the die attach layer has a thickness of between about 5 and 7 mils.

11. The integrated circuit package of Claim 8, wherein the die attach layer is an epoxy modified with elastomeric material.

a10

12. (Amended) The integrated circuit package of Claim 8, wherein the array is a ball grid array.

13. (Amended) The integrated circuit package of Claim 8, wherein the array is a tape ball grid array.

14. (Amended) The integrated circuit package of Claim 8, wherein the array is a micro ball grid array.

15. An integrated circuit package, comprising:

a die;

a die attach layer over the die; and

an array of solder balls over the die attach layer;

wherein the die attach layer has a coefficient of thermal expansion of less than about 106 ppm/°C and a modulus of elasticity of less than about 126 ksi.

a11

16. (Amended) The integrated circuit package of Claim 15, further comprising a flexible tape connecting the array of solder balls to the die, wherein one end of the tape is located over the die attach layer, and another end of the tape is located over the die.

17. (Amended) A first level integrated circuit package, comprising:

a first level package including a chip;

an array of solder balls for connecting the first level package to a second level package;

an adhesive layer between the chip and the array of solder balls, the adhesive layer having a coefficient of thermal expansion of less than about 200 ppm/°C; and

a flexible tape connecting the array to the chip

wherein one end of the tape is located over the adhesive layer, and another end of the tape is located over the chip.

18. The package of Claim 17, wherein the tape connects the array to the chip using μBGA technology.

19. The package of Claim 17, wherein the adhesive layer has a coefficient of thermal expansion of less than about 150 ppm/°C.

20. The package of Claim 17, wherein the adhesive layer has a coefficient of thermal expansion of less than about 100 ppm/°C.

a12

21. (Amended) A first level integrated circuit package, comprising:

a first level package including a chip;

an array of solder balls for connecting the first level package to a second level package;

an adhesive layer between the chip and the array of solder balls, the adhesive layer having a coefficient of thermal expansion of less than about 200 ppm/°C; and

a flexible tape connecting the array to the chip;

wherein the adhesive layer has a modulus of elasticity of greater than about 10 ksi and less than about 126 ksi.

22. The package of Claim 21, wherein the adhesive layer has a modulus of elasticity of greater than about 50 ksi.

23. The package of Claim 22, wherein the adhesive layer has a modulus of elasticity of greater than about 100 ksi.

A13

25. (Amended) An integrated circuit package, comprising:

a flexible substrate;

a chip;

a plurality of conductive terminals on the substrate;

a plurality of conductive leads electrically connecting the conductive terminals to the chip; and

a compliant material between the chip and the substrate, the compliant material having a modulus of elasticity of less than about 126 ksi at room temperature and a coefficient of thermal expansion of less than about 200 ppm/°C.

26. The integrated circuit package of Claim 25, wherein the plurality of conductive terminals includes an array of solder balls.

27. The integrated circuit package of Claim 25, wherein the plurality of conductive leads includes TAB leads.

Please add the following new claim:

A14

28. (New) The integrated circuit package of Claim 25, wherein the flexible substrate is a polyimide.

REMARKS

With this amendment Claims 8-23 and 25-28 are pending in the present application. Claims 1-7 and 24 have been canceled without prejudice. Applicant reserves the right to pursue these claims at a later date. Claims 9, 12-14, 16, 17, 21 and 25 has been amended, and Claim 28 has been added to correct the typographical error of the original Claim 25. The specific changes to the specification and to the amended claims are shown on a separate set of pages attached hereto and entitled VERSION WITH MARKINGS TO SHOW CHANGES MADE, which follows the signature page of this Amendment. On this set of pages, the insertions are underlined while the [deletions are in brackets]. In view of the foregoing amendments and the following remarks, Applicant respectfully requests reconsideration and allowance of this application.

Objections to the Drawings

The Examiner objected to the drawings, asserting that the Figures are improperly crosshatched. Appropriate corrections have been made and are attached on a separate set of pages following the page entitled Proposed Drawing Changes.

The drawings were also objected to because, in Figure 1C, the thick layer of adhesive material is labeled with reference number 80, which is used to label a thin layer of adhesive material. The Examiner also asserts that in Figure 2, the thick layer of adhesive is labeled with reference number 80, which is used to label a thin layer of adhesive material. The Examiner further asserts that it is not clear where Figure 2 ends, because there are no lines at the right portion of the Figure. Appropriate corrections have been made and are attached on a separate set of pages following the page entitled Proposed Drawing Changes.

The drawings have also been objected to as failing to comply with 37 CFR 1.84(p)(5). The Examiner asserts that reference number 88 appears in the drawings, but is not mentioned in the description. Applicant respectfully notes that reference number 88 is in fact used on page 7, line 26 to refer to "solder pads 88."

Objections to the Specification:

The disclosure has been objected to because on page 5, line 30 the reference number 50 is called "leads," while on page 8, lines 13-15, it is called "tape." The Examiner further

asserts that on page 8, lines 3 and 20 the reference number 80 is called "die attachment layer," while on page 5, line 25 it is called "thin layer of adhesive material."

As indicated above, the specification and drawings have been amended to include reference number 50' to refer to the "tape." The specification and drawings have also been amended to refer to the "die attachment layer" with reference number 80'. Accordingly, Applicant respectfully requests that these objections be withdrawn.

Claim Objections

Claim 25 was objected to. The sentence "The integrated circuit package of Claim 25, wherein the flexible substrate is a polyimide" at the end of claim 25 has been deleted from Claim 25 and added as Claim 28, as suggested by the Examiner. Accordingly, Applicant respectfully requests that this objection be withdrawn.

Claim Rejections - 35 U.S.C. § 112

Claims 9, 12-14, 16-20, 21-23, 26, and 27 have been rejected under 35 U.S.C. § 112, second paragraph, as being indefinite. In particular, the Examiner asserted that Claims 9 and 16 were rejected as being incomplete for omitting essential structural cooperative relationships of elements. Specifically, the Examiner asserts that the location of the flexible tape relative to the die and the die attach layer is omitted.

Claims 9 and 16 have been amended as indicated above to include the location of the flexible tape relative to the die and the die attach layer. Thus Applicant respectfully requests that these rejections be withdrawn.

The Examiner also asserts that Claims 12-14, and 18 are unclear regarding whether the ball grid array, the tape ball array and the micro ball array are separate from the original array of solder balls of Claim 8, or whether there are two pluralities of solder balls. Applicant respectfully points out that Claim 18 is in no way related to Claim 8, and therefore does not include the original array of solder balls recited in Claim 8 as stated by the Examiner. Thus the rejection of Claim 18 as indefinite appears to be moot. Claims 12-14 have been amended as indicated above, and thus, Applicant respectfully requests that the rejections be withdrawn.

The Examiner asserts that Claim 17 lacks antecedent basis for the limitation, "the first level package." Applicant has amended Claim 17 to include a recitation of "a first level package."

The Examiner further asserts with respect to Claim 17, that it is not clear how the chip is connected to a first level package or if the chip is the first level package, and how a first level package can comprise a second level package and still have the adhesive layer in between the chip and the array of solder balls. The Examiner further asserts that it is unclear how the flexible tape is located in relation to the other elements of the package, such as the ball array and the adhesive layer.

Claim 17 has been amended to clarify the structural and geographic relationships of the elements of that claim. Applicant therefore respectfully requests that the rejection be withdrawn.

The Examiner asserts that the limitation "the first level package" in line 3 of Claim 21 lacks antecedent basis. Claim 21 has been amended as indicated above. Thus, Applicant respectfully requests that the rejection be withdrawn.

The Examiner asserts that Claims 26 and 27 are unclear regarding whether the conductive terminals are solder balls, or if the balls are a separate piece connected to the terminals. Applicant respectfully submits that Claim 26 is clear as written. Claim 26 recites, among other limitations, "a plurality of conductive leads electrically connecting the conductive terminals to the chip," "wherein the plurality of conductive terminals includes an array of solder balls." Applicant respectfully submits that the Examiner has merely pointed out two possible embodiments of these limitations of an integrated circuit package as claimed. Applicant further submits that there is nothing unclear or indefinite about the fact that the limitations of a claim may include more than one possible embodiment. Applicant submits that Claim 27 is also clear and definite, although the Examiner's assertion does not seem to be relevant due to the fact that Claim 27 does not include limitations specifically directed toward, "conductive terminals" and "solder balls" beyond the fact that Claim 27 is dependent on Claim 25. Thus, Applicant respectfully requests that the rejection be withdrawn.

Claim Rejections 35 U.S.C. § 103

Claims 8, 10-16 have been rejected under 35 U.S.C. § 103(a) as being unpatentable over Hsuan et al. (US Patent No. 6,239,367).

Regarding Claims 8 and 15, the Examiner asserts that Hsuan et al. teaches an integrated circuit package, comprising: a die (56); a die attach layer (76) over the die; and an array of solder balls (72) over the die attach layer. The Examiner further asserts that Hsuan fails to explicitly teach the die attach layer having a coefficient of thermal expansion of less than about 106 ppm/°C, and a modulus of elasticity of less than about 126 ksi. The Examiner asserts that it is well known in the art to use different adhesive materials according to the desired properties needed to manufacture and use the device, and that it would have been obvious to one of ordinary skill in the art at the time of the invention to use the adhesive having the set of properties desired since it has been held to be within the general skill of a worker in the art to select a known material on the basis of its suitability for the intended use as a matter of obvious design choice. The Examiner further asserts that it has been held that discovering an optimum value or range of a result effective variable involves only routine skill in the art.

Applicant traverses the rejection and respectfully submits that the Examiner has not established a *prima facie* case of obviousness. In order to establish a prima facie case of obviousness, *all* the claim limitations must be taught or suggested by the prior art relied upon. Applicant respectfully submits that nowhere does Hsuan teach or suggest an adhesive having the properties recited in Applicant's Claims 8 and 15. Applicant submits that one skilled in the art would not have known to use an adhesive having a coefficient of thermal expansion of less than about 106 ppm/°C in an integrated circuit package as recited in Applicant's Claim 8, because the importance of this property was not recognized by Hsuan. Moreover, Applicant submits that that the Examiner has not pointed to any reference which indicates that a die attach layer having the properties recited in Claims 8 and 15 was known to those skilled in the art.

As described in the specification of the above-identified application, at page 2, line 22 through page 3, line 5, the prior art has generally used die attach layers having a low modulus of elasticity, and a high coefficient of thermal expansion. Because of the die attach layer's

high coefficient of thermal expansion and compliance relative to the die, the die attach layer expands and shrinks more rapidly than the die during thermal exposure. This creates stress on the conductive leads connecting the solder ball array to the die, and causes breakage of the leads from the die. By recognizing the relationship between these properties of the die attach layer as compared to those of a typical die, and by providing an integrated circuit package using a die attach layer with substantially different properties from those of die attach layers of the prior art, Applicant has provided an integrated circuit package with a substantially reduced tendency to suffer from the problem known as heal break.

Applicant respectfully submits that nowhere does Hsuan discuss the problem of heal break, nor does Hsuan suggest changing the properties of the die attach layer to address such a problem. Furthermore, the Examiner has not provided any reference indicating that a die attach layer as claimed was known. Applicant therefore submits that providing a die attach layer having a coefficient of thermal expansion of less than about 106 ppm/°C as recited in Claims 8 and 15 is much more than a mere design choice, and therefore it would not have been obvious to one of skill in the art at the time of the invention to provide an integrated circuit package as recited in either Claim 8 or Claim 15 based on Hsuan et al.

Moreover, Applicant respectfully disagrees with the characterization of these limitations as being simply "optimum" ranges. Applicant submits that a rejection based on "optimum or workable ranges" is inappropriate where the prior art does not teach or suggest the desirability of the result achieved. As discussed in MPEP § 2144.05, "[a] particular parameter must first be recognized as a result-effective variable, i.e., a variable which achieves a recognized result, before the determination of the optimum or workable ranges of said variable might be characterized as routine experimentation." In re Antonie, 559 F.2d 618, 195 U.S.P.Q. 6 (CCPA 1977). Thus, for a rejection to be made based on "optimum or workable ranges," the prior art must first identify the result which the variable achieves.

As discussed above, in one embodiment of the above-identified application, the problem of thermally induced heal break can be substantially eliminated by providing a die attach layer with a coefficient of thermal expansion less than about 200 ppm/°C. Nowhere does Hsuan teach or suggest the desirability of varying either the coefficient of thermal expansion or the modulus of elasticity, in addressing the problem of heal breakage.

Accordingly, without disclosing this desired result, Hsuan et al. cannot be used to reject the claims on the basis that the parameters affecting this result are merely "optimum or workable" ranges that would be known to one of skill in the art. Thus, Applicant respectfully requests that the rejections of Claims 8 and 15 be withdrawn.

Claims 9-14 and 16 depend from Claims 8 and 15 respectively. As such Claims 9-14 and 16 include the unique combinations of limitations of their respective base claims as well as some additional unique features also not taught or suggested by the prior art of record. Thus Applicant respectfully requests that the rejection be withdrawn.

Claims 17-23 have been rejected under 35 U.S.C. § 103(a) as being unpatentable over DiStefano (U.S. Patent No. 6,127,724). Regarding Claim 17 and 21, the Examiner asserts that DiStefano teaches a first level integrated circuit package comprising a chip (32), an array of solder balls (62), an adhesive layer (50) between the chip and the array of solder balls, and a flexible tape (20) connecting the array to the chip. The Examiner asserts that DiStefano fails to teach that the adhesive layer has a coefficient of thermal expansion of less than about 200 ppm/°C and wherein the adhesive layer has a modulus of elasticity of greater than about 10 ksi and less than about 126 ksi. The Examiner asserts that it is well known in the art to use different adhesive materials according to the desired properties needed to manufacture and use the device, and that it would have been obvious to one of ordinary skill in the art at the time of the invention to use the adhesive having the set of properties desired since it has been held to be within the general skill of a worker in the art to select a known material on the basis of its suitability for the intended use as a matter of obvious design choice. The Examiner further asserts that it has been held that discovering an optimum value or range of a result effective variable involves only routine skill in the art.

Applicant traverses the rejection and the Examiner's characterization of the cited reference. Applicant respectfully submits that the Examiner has not established a *prima facie* case of obviousness. In order to establish a prima facie case of obviousness, *all* the claim limitations must be taught or suggested by the prior art relied upon.

Applicant respectfully submits that nowhere does DiStefano teach or suggest an adhesive having the properties recited in Applicant's Claims 17 and 21. Applicant submits that one skilled in the art would not have known to use an adhesive having a coefficient of

thermal expansion of less than about 200 ppm/°C in an integrated circuit package in combination with the other features recited in Applicant's Claim 17, because the importance of this adhesive property was not recognized by DiStefano, nor has the Examiner pointed out that such an adhesive was actually known.

As described above, by recognizing the relationship between these properties of the die attach layer as compared to those of a typical die, and by providing an integrated circuit package using a die attach layer with substantially different properties from those of die attach layers of the prior art, Applicant has provided an integrated circuit package with a substantially reduced tendency to suffer from the problem known as heal break.

Applicant respectfully submits that nowhere does DiStefano suggest changing the properties of the die attach layer to allow the layer to expand or contract during thermal variations with the die. The feature identified by the Examiner as a die attach layer is in fact a post, as indicated at Column 7, lines 8-17. DiStefano states that "posts 50 are formed from a thermally and electrically conductive material. For example, a die attach adhesive such as a silver-filled epoxy... can be used. Posts should be flexible enough to accommodate displacements of the magnitude which will be caused by thermal expansion of the chip relative to surrounding components."

Applicant therefore submits that providing a die attach layer having a coefficient of thermal expansion of less than about 200 ppm/°C as recited in Claims 17 and 21 is more than a mere design choice, and therefore it would not have been obvious to one of skill in the art at the time of the invention to provide an integrated circuit package as recited in either Claim 17 or Claim 21 based on DiStefano.

Moreover, Applicant respectfully disagrees with the characterization of these limitations as being simply "optimum" ranges. Applicant submits that a rejection based on "optimum or workable ranges" is inappropriate where the prior art does not teach or suggest the desirability of the result achieved. As discussed in MPEP § 2144.05, "[a] particular parameter must first be recognized as a result-effective variable, i.e., a variable which achieves a recognized result, before the determination of the optimum or workable ranges of said variable might be characterized as routine experimentation." In re Antonie, 559 F.2d

618, 195 U.S.P.Q. 6 (CCPA 1977). Thus, for a rejection to be made based on "optimum or workable ranges," the prior art must first identify the result which the variable achieves.

As discussed above, in one embodiment of the above-identified application, the problem of thermally induced heal break can be substantially eliminated by providing a die attach layer with a coefficient of thermal expansion less than about 200 ppm/°C. Nowhere does DiStefano teach or suggest the desirability of a low coefficient of thermal expansion for the die attach layer in addressing the problem of heal breakage. Accordingly, without disclosing this desired result, DiStefano cannot be used to reject the claims on the basis that the parameters affecting this result are merely "optimum or workable" ranges that would be known to one of skill in the art. Thus, Applicant respectfully requests that the rejections be withdrawn.

Claims 18-20, 22, and 23 depend from Claims 17 and 21, respectively. As such, Claims 18-20, 22, and 23 include the unique combinations of limitations of their respective base claims as well as some additional unique features also not taught or suggested by the prior art of record. Thus Applicant respectfully requests that the rejection be withdrawn.

Claims 25-27 have been rejected under 35 U.S.C. § 103(a) as being unpatentable over Kovac et al. (U.S. Patent No. 5,659,952). The Examiner asserts that Kovac teaches an integrated circuit package comprising a flexible substrate (100), a chip (120), a plurality of conductive terminals (140) on the substrate, a plurality of conductive leads (150) electrically connecting the conductive terminals to the chip, and a compliant material (170) between the chip and the substrate.

Applicant traverses the rejection and respectfully submits that the Examiner has not established a *prima facie* case of obviousness. Applicant respectfully submits that nowhere does Kovac teach or suggest a compliant material having the properties recited in Applicant's Claim 25. Applicant submits that in view of Kovac, one skilled in the art would not have known to use a compliant material having a coefficient of thermal expansion of less than about 200 ppm/°C and a modulus of elasticity of less than about 126 ksi in an integrated circuit package, in combination with the other features recited, because the importance of these properties was not recognized. Moreover, Applicant submits that the Examiner has not shown that a compliant having the recited properties was known to those skilled in the art.

Applicant therefore submits that providing a compliant material having a modulus of elasticity of less than about 126 ksi at room temperature and a coefficient of thermal expansion of less than about 200 ppm/°C as recited in Claim 25 is more than a mere design choice, and therefore it would not have been obvious to one of skill in the art at the time of the invention to provide an integrated circuit package as recited in Claim 25 in view of Kovac.

Moreover, Applicant respectfully disagrees with the characterization of these limitations as being simply "optimum" ranges. Applicant submits that a rejection based on "optimum or workable ranges" is inappropriate where the prior art does not teach or suggest the desirability of the result achieved. As discussed in MPEP § 2144.05, "[a] particular parameter must first be recognized as a result-effective variable, i.e., a variable which achieves a recognized result, before the determination of the optimum or workable ranges of said variable might be characterized as routine experimentation." In re Antonie, 559 F.2d 618, 195 U.S.P.Q. 6 (CCPA 1977). Thus, for a rejection to be made based on "optimum or workable ranges," the prior art must first identify the result which the variable achieves.

As discussed above, in one embodiment of the above-identified application, the problem of thermally induced heal break can be substantially eliminated by providing a compliant material with a coefficient of thermal expansion less than about 200 ppm/°C. Nowhere does Kovac teach or suggest the desirability of varying either the coefficient of thermal expansion or the modulus of elasticity in addressing the problem of heal breakage. Accordingly, without disclosing this desired result, Kovac et al. cannot be used to reject the claims on the basis that the parameters affecting this result are merely "optimum or workable" ranges that would be known to one of skill in the art. Thus Applicant respectfully requests that the rejection of Claim 25 be withdrawn.

Claims 26 and 27 depend from Claim 25. As such Claims 26 and 27 include the unique combinations of limitations of their base claim as well as some additional unique features also not taught or suggested by the prior art of record. Thus, Applicant respectfully requests that the rejections be withdrawn.

CONCLUSION

In view of the foregoing amendments and remarks, Applicant submits that this application, as amended, is in condition for allowance and such action is respectfully requested. The undersigned has made a good faith effort to respond to all of the rejections and objections in the case, and to place the claims in condition for immediate allowance. Nevertheless, if any undeveloped issues remain or if any issues require clarification, the Examiner is respectfully requested to call Applicant's counsel at the number indicated below in order to resolve such issues promptly.

Respectfully submitted,

KNOBBE, MARTENS, OLSON & BEAR, LLP

Dated: 3-8-02

By: _____

Sabing H. Lee
Registration No. 43,745
Attorney of Record
620 Newport Center Drive
Sixteenth Floor
Newport Beach, CA 92660